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Résumé

EXPERIENCE

6 years

Sevni Technology, Los Altos Hills, CA
adVenture Planner

- Consultant to VC's and entrepreneurs on new technology development and directions
- Consultant to DARPA MTO on the search, evaluation, and development of new program ideas in electronic technology. Scoped a new program start in Asynchronous Logic and Software Support.
- Certified Information Systems Security Professional (CISSP #42433)
- *ACM Queue* – new publication in *Scientific American* style for the computer professional. Led *Storage Systems* issue; guided *Security*, *Embedded Systems*, and numerous other issues.

1 year

Intransa Inc., Sunnyvale, CA
Vice President, Engineering

Co-founder and chief architect of startup into storage systems.

- Co-developed, presented and sold business plan that resulted in \$17.5M 1st round funding from USVP, ATV Capital, and 3Com during nuclear winter of funding. Developed a differentiating architecture from vague initial product ideas. Came up to speed with storage and networking issues, interviewed customers, and conducted feasibility studies. Organized rapid prototype development while bringing on initial hires in first 10 weeks. Developed budget and plan for one year, 49 person initial effort. Personally developed and wrote architecture spec. Personally wrote and implemented hiring plan. Trained engineering hires to focus on quality staff hires. Recruited team; 17 direct reports (of 20 people in company). Specified engineering computing environment.

5 years

Synopsys Inc., Mountain View, CA
Director of Research, Advanced Technology Group

Established embedded systems research group focusing on 3 to 5 year out compiler and related technology development.

- Conceived, developed, and managed the acclaimed Nimble C Compiler project that targeted a reconfigurable datapath coprocessor and standard processor. Two patents; numerous discoveries. New algorithms in C code transformations, HW/SW partitioning, and datapath compilation developed. . Developed the contacts and led a collaboration with UC Berkeley, LM Advanced Technology Laboratories, National Semi and Technical University of Braunschweig. Staffed to 5 senior, post-doc researchers in-house and team of 12 engineers overall. Sought and received \$4.5M of outside funding over 2.5 years.
- *Served on DAC Executive Committee as New Initiatives Chair. Served on Technical Program Committee (3 years), Panel Committee (2 years). Served on numerous NSF and DARPA advanced studies. Wrote 1999 ITRS Systems Design section; one of 15+ members of 1997 and 1999 NTRS/ITRS (SIA Technology Roadmap for Semiconductors) design section. Co-editor of IEEE Computer special issue on Reconfigurable Computing (April 2000).*
- Managed computer systems for ATG and was liason to corporate IT department; major effort on Y2K transition.

Program Manager and Senior Scientist, Logic Modeling Group

Established advanced technology group under CTO to develop future technology and industry standards activity.

- Staffed and led technical development on two efforts: development of MCM bare die interchange standard (EIA DIE standard) and IC behavioral model generators. Obtained and managed \$3M in DARPA funding for efforts.
- *Founded and led for twelve years the eda.org / vhdl.org internet services (ISP content, services and dial-up network) as a personal initiative. Served on the VHDL International Board of Directors. Founded VHDL Users' Group and grew to 1500 members worldwide.*

3 years

Defense Advanced Research Projects Agency, Arlington, VA**Program Manager, Electronics Technology Office**

Defined and implemented investment strategy for electronics and software research with a focus on design technology and signal processing. Served term appointment.

- Developed office strategy on mixed-technology integration that joined efforts of biological, RF, fluidic, and Sense/Actuate systems on single chips. Led to the renaming of the office and creation of a congressional line item (PE 0603739E Project MT-15) which has expanded to more than \$600M expended to date and a continued expansion in scope and scale.
- Initiated and led industry in development of design tools for and concept of single chip mixed analog, digital, and microelectromechanical (MEMS) systems (Mixed Technology Integration, \$55M, 4 years).
- Negotiated and successfully setup a novel R&D agreement for the creation of a new microwave and millimeter wave design environment (MAFET, \$70M, 5 years).
- Half way through, realigned into a multi-board, DSP focus and brought to a successful close the Rapid prototyping of Application Specific Signal Processors program (RASSP, \$150M, 4 years).
- Initiated and led several blue ribbon workshops and panels on design technology, signal processing software, and wireless sensors. Participated in agency wide studies into next generation Internet Technology and Information warfare.

2 years

Aspect Development, Los Altos, CA**Director of Software Development**

- Only engineering manager for first year of company. Started consulting 1 year before with founder to develop ideas before joining as 3rd on staff. Supervised development of client-server database, data (re)sourcing products, VHDL model libraries, and database authoring tools. Managed engineering group of 25 in Bangalore, India and 10 in Los Altos, CA.

EDUCATION**M.S.E. and B.S.E., Computer Engineering**

Case Western Reserve University, Cleveland, OH; and University of Edinburgh, Edinburgh, Scotland. Computer Graphics and E.D.A. specialization; Minor, Economics. IBM Yorktown Heights Doctoral Fellow.

- Specified and developed CCORE - a device independent, interactive graphics software package for use in cartography and C.A.E. applications (50k+ lines) (NSA grant; NSA user)
- Co-Developed CHEMLAB-II -- a design automation tool for molecular analysis and design (200k + lines) (CWRU Macromolecular Department, NIH grant; eventually sold to Macromolecular Modeling and sold until 1996)

PERSONAL

Married with family. Soccer Referee. Enjoy bike riding, skiing and travel. Private Pilot.

References available upon request